Amendments to the Specification

Please insert the following new paragraph at page 1, line 9 (immediately before Field of the Invention):

This is a divisional of application Serial No. 09/653,513, filed August 31, 2000, (pending), which is incorporated herein by reference.

Please replace the paragraph beginning at page 8, line 24, with the following amended paragraph.

Figure 1 is a scanning electron [[microcraph]]micrograph of a platinum film deposited at a thickness of less than 500 Angstroms on silicon after rapid thermal oxidation at 700°C and atmospheric pressure for 1 minute.

Please replace the paragraph beginning at page 12, line 6, with the following amended paragraph.

A preferred platinum-zirconium film may be formed by vapor deposition from precursor compounds (typically, organometallic precursor compounds), as opposed to physical deposition (e.g., sputtering) techniques, because of the ability of these methods to form conformal layers. That is, vapor deposition techniques are desired because they are more suitable for deposition on semiconductor substrates or substrate assemblies, particularly in contact openings which are extremely small and require conformally filled layers of metal. Such methods typically involve various forms of chemical vapor deposition (CVD), for example, atmospheric pressure chemical vapor deposition, low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or any other chemical vapor deposition technique. Another vapor deposition technique called atomic layer deposition (ALD) can also be used. This method involves the formation of a monomolecular layer of a precursor compound, which is then contacted with a reaction gas, as disclosed in [[Vacuum Technology and Coating, May 2000, page 33]]Pathangey et al., "Atomic Layer Deposition for Nanoscale Thin Film Coatings", Vacuum Technology and Coating, pages 32-41, May 2000. A preferred deposition process includes the use of separate platinum and zirconium precursors, although one compound could be envisioned to provide both metals.

Please replace the paragraph beginning at page 21, line 19, with the following amended paragraph.

Alternatives to such methods include an approach wherein the precursor composition is heated and vapors are drawn off and controlled by a vapor mass flow controller, and a pulsed liquid injection method as described in "Metalorganic Chemical Vapor Deposition By Pulsed Liquid Injection Using An Ultrasonic Nozzle: Titanium Dioxide on Sapphire from Titanium (IV) Isopropoxide," by Versteeg, et al., Journal of the American Ceramic Society, 78, 2763-2768 (1995). The complexes described herein are also particularly well suited for use with vapor deposition systems, as described in copending application U.S. Serial No. 08/720,710 entitled "Method and Apparatus for Vaporizing Liquid [[Precursor compositions]]Precursors and System for Using Same," filed on October 2, 1996. Generally, one method described therein involves the vaporization of a precursor composition in liquid form (neat or solution). In a first stage, the precursor composition is atomized or nebulized generating high surface area microdroplets or mist. In a second stage, the constituents of the microdroplets or mist are vaporized by intimate mixture of the heated carrier gas. This two stage vaporization approach provides a reproducible delivery for precursor compositions (either in the form of a neat liquid or solid dissolved in a liquid medium) and provides reasonable growth rates, particularly in device applications with small dimensions.

Please replace the paragraph beginning at page 24, line 11, with the following amended paragraph.

Referring to Fig. 12, the portion of the conductive layer 152 above the top of the BPSG layer 142 is removed through a planarization process, thereby electrically isolating the portions of layer 152 remaining in the bit line contact opening 144 and capacitor openings 146.

Referring now to Fig. [[134]]13, a capacitor dielectric layer 154 is provided over conductive layer 152 and capacitor openings 146.

Please replace the paragraph beginning at page 25, line 2, with the following amended paragraph.

Referring to Fig. [[13]]14, the second conductive layer 156 and underlying capacitor dielectric layer 154 are patterned and etched such that the remaining portions of each group of the first conductive layer 152, capacitor dielectric layer 154, and second conductive layer 156 over the bit line contact opening 144 and capacitor openings 146 are electrically isolated from each other. In this manner, each of the active areas 116, 118, 120 are also electrically isolated (without the influence of the gate). Furthermore, at least a portion of the barrier layer 151 and the first conductive layer 152 in contact with the plug 150 over the bit line active area 118 are outwardly exposed.

Please replace the paragraph beginning at page 25, line 11, with the following amended paragraph.

Referring now to Fig. [[14]]15, a bit line insulating layer 158 is provided over the second conductive layer 156. The bit line insulating layer 158 is preferably comprised of BPSG. The BPSG is typically reflowed by conventional techniques, i.e., heating to about 800°C. Other insulating layers such as PSG, or other compositions of doped SiO_2 may similarly be employed as the insulating layer 158.